A Naval Energy Efficient Synthesis of Full Adder

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ABSTRACT: *In Electronic device adder has been used frequently. An adder is specified in terms of delay area and power. This paper suggests a possible method for reduction in power Software used for simulation of adder is Mentor graphics with 180 nm technology. By comparing proposed adder with existing adders reduction in power delay product has been found.*

Keywords – *Hybrid flow adder, PMOS, NMOS.*

1. INTRODUCTION

In VLSI design various factors effecting thedesign are cost, delay and power consumption, now a days power consumption plays very important role. Adder is the basic building block in design of digital circuits; hence it plays an important role in determining the overall response of digital design. Increasing the performance of adder is important for enhancing the specification of design.By improving specification like power, delay, size of transistor and capacitance performance is greatly improved. [1], [2].Mainly three type of power dissipation occurred in circuits. These are as following:

1. Leakage Power: Power flow when transistor is off.

2. Short Circuit Power: When their exist a direct path between supply and ground.

3. Switching Power: Due to alternate charging discharging of capacitor.

This paper contains 6 sections. Section I introduction about adder. Second section describes approachabout existing adders merits and demerits. In section three, Low count transistorare discussed. Section IV contains proposed models. In next two sessions results and conclusions are discussed.

Adder is used to add two numbers. At first adder circuits were designed with static CMOS technology as given in Fig. 1. It includes certain advantages like easy to operate at small voltage and easy to resize the transistor [3]. I uses equal number of transistor i.e NMOS and PMOS, therefore area requirement increases. To overcome this problem domino logic has been used [4]. Dynamic logic circuit technique requires a single clocked devices and it uses pull-up network or pull down network for implementation of circuits. Charge sharing problem may occur. To overcome this problem, a new technique i.e. domino logic has been suggested. The combination of dynamic circuits and static circuits commonly known as Domino gate [5].

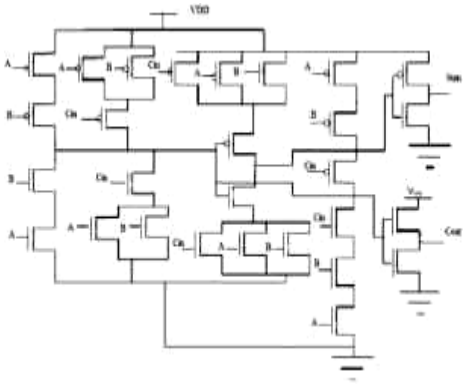

Fig. 1: Static CMOS Adder Circuit.

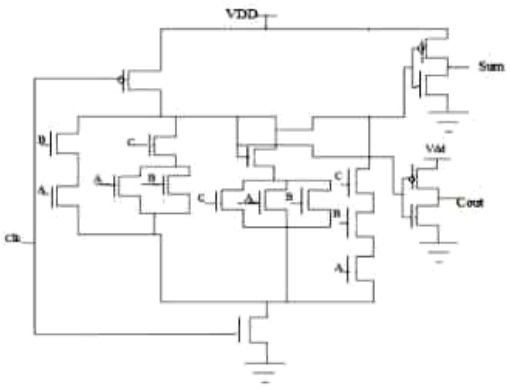

Fig. 2: Domino Logic Full Adder.

The figure of full adder based on dominology is given in Fig. 2. These circuits are faster and consume less power hence energy efficient but the main problem with this technique is use of common clock which makes it slightly slower for multi level digital circuits [6].

Low Transistor Count Full Adder:

Two transistors which come in pass transistor logic family are 10T and 14T. 10 T adders require least number of transistors i.e. PMOS and NMOS. Hence some times they are also called as low count transistor as given in fig. 3 [5].Transistor using more than one type of technology are called hybrid adders. Low count transistor logic suffer from strong and weak passage of signal, hence they can not give either full voltage VDD or 0 voltage or ground.

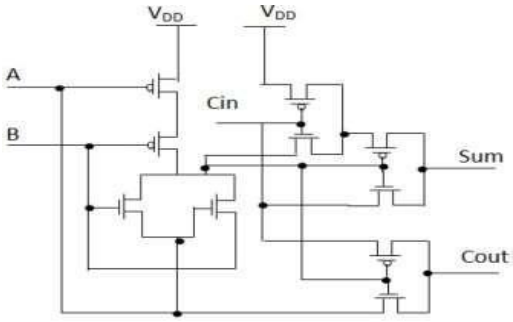

Fig. 3: 10 T adder circuit.

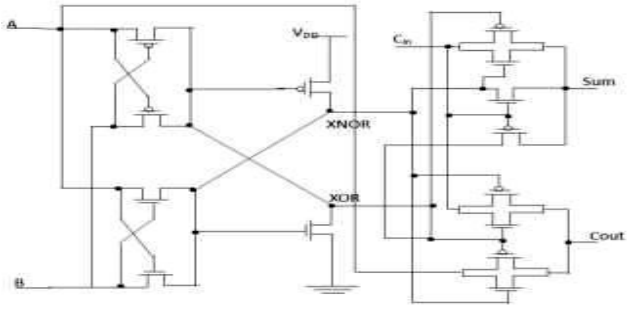

Fig. 4: 14 T Adder Circuit.

Second type of low count transistor is 14 Twhich requires only 14 transistorfor designing of full adder. They can produce XOR/XNOR function simultaneously, hence delay will decrease and a describable power delay product can be obtained. They also suffer from the problem of voltage drop like 10 T does [7, 8].

II. PROPOSED HYBRIDFLOW ADDER

Figure 5 explains module 1[8]. Its main disadvantage is threshold voltage drop. Its main problem occurs for the transition of AB as it changes from 01 to 00.

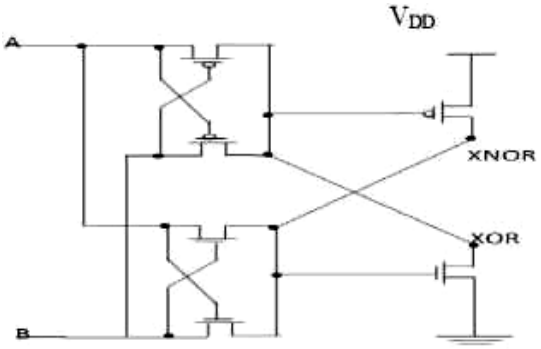

Fig. 5: Module 1 of adder circuit.

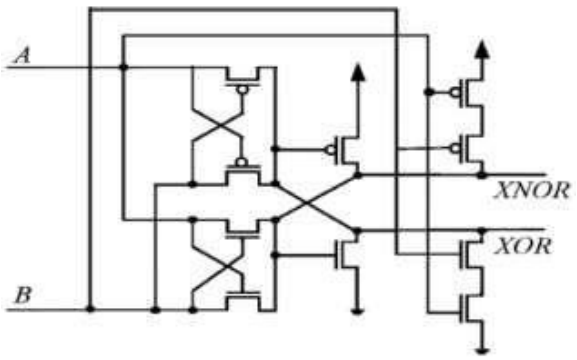

Fig. 6: Modified Module 1 circuit.

At low supply voltage is performance of above circuits is not good. To overcome the problem of above side threshold voltage drop came be overcome by using two transistors i.e. PMOS and NMOS connected in series as given in figure 6, which is modified module 1. Two series NMOS will solve the problem of 10 to 11 transition and two series PMOS will solve the problem of 01 to 00 transitions as now threshold voltage drop problem is compensated, hence full swing voltage is available at the output. With the introduction of this new technique power delay product is minimize upto a large extent as given in Fig. 5 is modified to Fig 6. By using multiplexer based on passedtransistor logic carry and sum output can be obtained as given in Fig. 7 and 8 respectively. The results and circuit diagrams of each adder described above is shown in the next section.

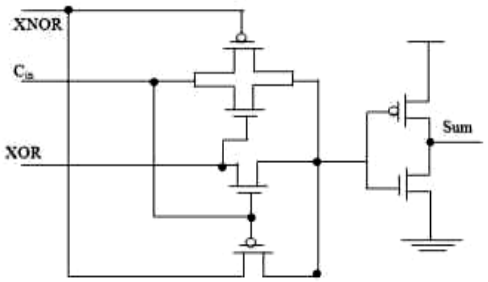

Fig. 7: Module 2 for adder circuit.

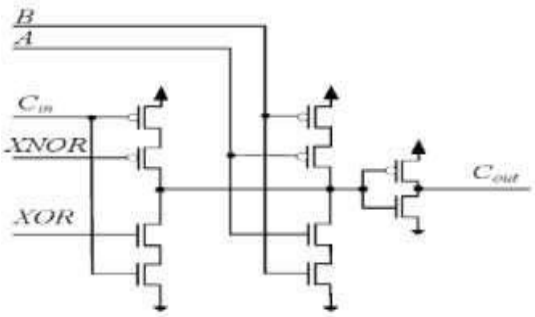

Fig.8: Module 3 for adder circuit.

Module 2 can be designed with static CMOS logic It uses six transistor for module 2There are several choices for Module 2 [7, 9].By using multiplexer carry output can be generated which is explained in module 3 [10]. Combining all three modules of adder as in fig. 9.

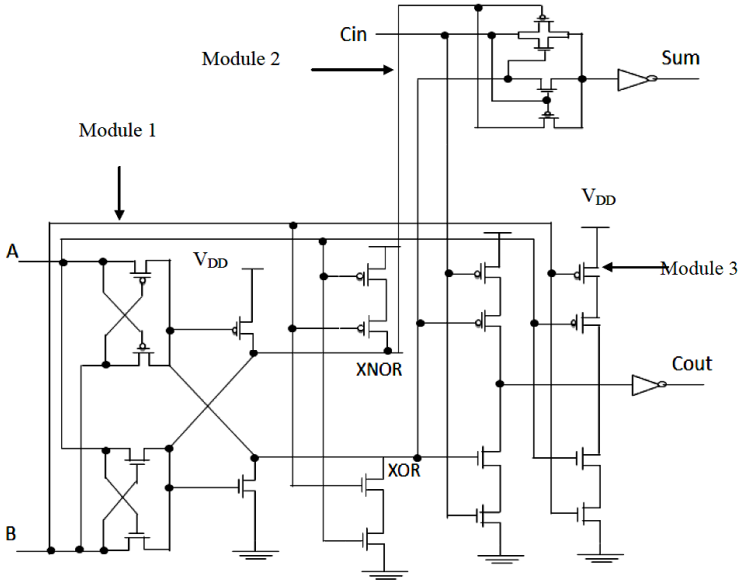

Fig. 9: Modified Hybrid full adder.

III. RESULT

All above explained adders are designed and simulation was done by mentor graphic on design Architect in 180nm. Voltage supply used is 1.8 V. Threshold voltages for NMOS and PMOS used is 08 V and 0.4 V respectively, Next schematics of above said adders are given along with their sum and carry output. It is seen from the compression of all adders that proposed hybrid full adder have least power delay product thought lowest power is obtained for static CMOS technology and least delay is obtained for 10T transistor but power delay product is minimum for hybrid full adder hence proposed hybrid full adder energy efficient as shown in Fig. 10.

Table I Analysis of various full adders.

Adder		**Parameters**	
Name	**Power**	**Delay**	**PDP**
Static CMOS	15.782	109.796	1732.453
Domino	15.861	151.512	2403.131
10 T	12.652	110.363	1396.312
14 T	7.001	115.281	807.082
HYBRID	4.689	115.091	520.905

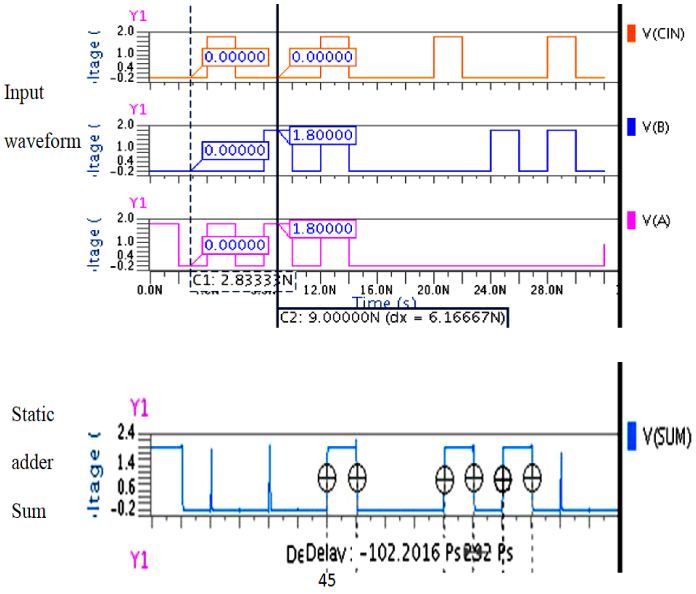

Fig. 10: Output waveforms depicting delay.

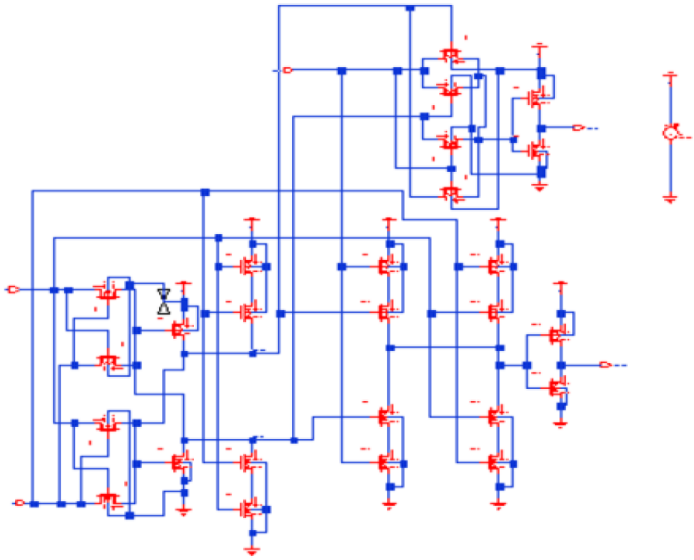

Fig. 11: Modified Hybrid Full Adder.

IV. CONCLUSION

Adder are widely used in VLSI, microprocessor etc. Thoroughly study of all existing adder and proposed hybrid adder had been done in this paper and from the result obtain it can be seen that proposed hybrid full adder have least propagation delay. Driving capability of hybrid full adder is more. For applications that required least power delay product, hybrid flow adder can be used there.

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